



Pipelined ADC Design and Enhancement Techniques [

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Monografía

Pipelined ADCs have seen phenomenal improvements in performance over the last few years. As such, when designing a pipelined ADC a clear understanding of the design tradeoffs, and state of the art techniques is required to implement today's high performance low power ADCs. Written for both researchers and professionals, Pipelined ADC Design and Enhancement Techniques provides: i.) A tutorial discussion, for those new to pipelined ADCs, of the basic design and tradeoffs involved in designing a pipelined ADC ii.) A detailed discussion of four novel silicon tested pipelined ADC topologies geared towards those looking to gain insight into state-of-the-art design in the area. The ADCs detailed include: - An 11-bit 45MS/s ADC which rapidly digitally calibrates in the background both DAC and gain errors - A 10-bit ADC with power scalable between 50MS/s (35mW) to 1kS/s (15 μ W) - A 10-bit ADC for use in sub-sampled systems with a technique to eliminate the front-end sample-and-hold - A 10-bit, 50MS/s ADC which uses a capacitive charge pump based approach to enable a very small power consumption of 9.9mW

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