Switched-Capacitor Techniques For High-Accuracy Filter And ADC Design [

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Springer Netherlands,
2007

Monografía

Switched capacitor (SC) techniques are well proven to be excellent candidates for implementing critical analogue functions with high accuracy, surpassing other analogue techniques when embedded in mixed-signal CMOS VLSI. Conventional SC circuits are primarily limited in accuracy by a) capacitor matching and b) the accuracy with which a differential amplifier can squeeze charge from one capacitor to another between clock periods. In Switched-Capacitor Techniques for High-Accuracy Filter and ADC Design, alternative SC techniques are proposed which allow the achievement of higher intrinsic analogue functional accuracy than previously possible in such application areas as analogue filter and ADC design. The design philosophy is to create the required functionality without relying on digital calibration or correction means but instead to develop methods which have reduced dependence on both component matching (especially capacitor matching) and parasitic effects (especially parasitic capacitance). However, the proposed techniques are just as amenable to further digital accuracy enhancement via calibration and/or correction as traditional methods. Two popular application areas are explored in the course of this book for exploitation of the proposed techniques, viz. SC filters and algorithmic ADCs - both cyclic and pipelined. Furthermore, efficient system level design procedures are explored in each of these two areas. The validity of the concepts developed and analyzed in Switched-Capacitor Techniques for High-Accuracy Filter and ADC Design has been demonstrated in practice with the design of CMOS SC bandpass filters and algorithmic ADC stages. For example, a 10.7MHz radio IF selectivity filter integrated in standard CMOS, employing the proposed methods, achieves an accuracy greater than ceramic filters. Another example is an ADC with better than 12-bit intrinsic accuracy, albeit capacitors with only 9-bits matching accuracy were used in the realization. The ADC architecture is also very robust and proven in an embedded digital VLSI application in the very newest 65nm CMOS. The power consumptions and silicon areas of the solutions proposed here are lower than other known solutions from the literature

Título: Switched-Capacitor Techniques For High-Accuracy Filter And ADC Design Recurso electrónico-En línea] by Patrick J. Quinn, Arthur H. M. Van Roermund

Editorial: Dordrecht Springer Netherlands 2007

Descripción física: XVIII, 244 p. digital

Tipo Audiovisual: Engineering Computer engineering Electronics Systems engineering Engineering Circuits and Systems Electronics and Microelectronics, Instrumentation Electrical Engineering

Mención de serie: Analog Circuits And Signal Processing Series

Documento fuente: Springer eBooks

Nota general: Engineering (Springer-11647)

Restricciones de acceso: Accesible sólo para usuarios de la UPV

Tipo recurso electrónico: Recurso a texto completo

Detalles del sistema: Forma de acceso: Web

ISBN: 9781402062582 978-1-4020-6258-2

Autores: Roermund, Arthur H. M. Van

Entidades: SpringerLink (Servicio en línea)

Enlace a formato físico adicional: Printed edition 9781402062575

Punto acceso adicional serie-Título: Analog Circuits And Signal Processing Series

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