Analysis and Design of Networks-on-Chip Under High Process Variation [

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Monografía

This book describes in detail the impact of process variations on Network-on-Chip (NoC) performance. The authors evaluate various NoC topologies under high process variation and explain the design of efficient NoCs, with advanced technologies. The discussion includes variation in logic and interconnect, in order to evaluate the delay and throughput variation with different NoC topologies. The authors describe an asynchronous router, as a robust design to mitigate the impact of process variation in NoCs and the performance of different routing algorithms is determined with/without process variation for various traffic patterns. Additionally, a novel Process variation Delay and Congestion aware Routing algorithm (PDCR) is described for asynchronous NoC design, which outperforms different adaptive routing algorithms in the average delay and saturation throughput for various traffic patterns. Demonstrates the impact of process variation on Networks-on-Chip of different topologies; Includes an overview of the synchronous clocking scheme, clock distribution network, main building blocks in asynchronous NoC design, handshake protocols, data encoding, asynchronous protocol converters and routing algorithms; Describes a novel adaptive routing algorithm for asynchronous NoC designs, which selects the appr opriate output path based on process variation and congestion

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Contenido: Introduction -- Network On Chip Aspects -- Interconnection -- Process Variation -- Synchronous And Asynchronous NoC Design Under High Process Variation -- Novel Routing Algorithm -- Simulation Results -- Conclusions

Detalles del sistema: Modo de acceso: World Wide Web

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