CMOS Single Chip Fast Frequency Hopping Synthesizers For Wireless Multi-Gigahertz Applications [Design Methodology, Analysis, and Implementation /

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Monografía

Recently, wireless LAN standards have emerged in the market. Those standards operate in various frequency ranges. To reduce component count, it is of importance to design a multi-mode frequency synthesizer that serves all wireless LAN standards including 802.11a, 802.11b and 802.11g standards. With different specifications for those standards, designing integer-based phase-locked loop frequency synthesizers can not be achieved. Fractional-N frequency synthesizers offer the solution required for a common multi-mode local oscillator. Those fractional-N synthesizers are based on delta-sigma modulators which in combination with a divider yield the fractional division required for the desired frequency of interest. In CMOS Single Chip Fast Frequency Hopping Synthesizers for Wireless Multi-Gigahertz Applications, the authors outline detailed design methodology for fast frequency hopping synthesizers for RF and wireless communications applications. Great emphasis on fractional-N delta-sigma based phase locked loops from specifications, system analysis and architecture planning to circuit design and silicon implementation. The book describes an efficient design and characterization methodology that has been developed to study loop trade-offs in both open and close loop modelling techniques. This is based on a simulation platform that incorporates both behavioral models and measured/simulated sub-blocks of the chosen frequency synthesizer. The platform predicts accurately the phase noise, spurious and switching performance of the final design. Therefore excellent phase noise and spurious performance can be achieved while meeting all the specified requirements. The design methodology reduces the need for silicon re-spin enabling circuit designers to directly meet cost, performance and schedule milestones. The developed knowledge and techniques have been used in the successful design and implementation of two high speed multi-mode fractional-N frequency synthesizers for the IEEE 801.11a/b/g standards. Both synthesizer designs are described in details

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