



Integrated Circuit and System Design. Power and Timing Modeling, Optimization and Simulation [18th International Workshop, PATMOS 2008, Lisbon, Portugal, September 10-12, 2008. Revised Selected Papers /

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 Arithmetic and Logic Structures Memory Structures Circuits and Systems

Monografía

This book constitutes the thoroughly refereed post-conference proceedings of 18th International Workshop on Power and Timing Modeling, Optimization and Simulation, PATMOS 2008, featuring Integrated Circuit and System Design, held in Lisbon, Portugal during September 10-12, 2008. The 31 revised full papers and 10 revised poster papers presented together with 3 invited talks and 4 papers from a special session on reconfigurable architectures were carefully reviewed and selected from numerous submissions. The papers are organized in topical sections on low-leakage and subthreshold circuits, low-power methods and models, arithmetic and memories, variability and statistical timing, synchronization and interconnect, power supplies and switching noise, low-power circuits; reconfigurable architectures, circuits and methods, power and delay modeling, as well as power optimizations addressing reconfigurable architectures

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